CLAIMS:

1. A time-of-flight (TOF) system integrated onto a single chip for measuring precise time intervals, said system comprising:

a first constant fraction discriminator for receiving an analog start signal input and providing a digital output representative of the start signal;

a second constant fraction discriminator for receiving an analog stop signal input and providing a digital output representative of the stop signal;

a logic circuit coupled with the first and second constant fraction discriminators for determining a Δt time interval between the start and stop signals; and

a time-to-digital converter (TDC) receiving as input the Δt time interval between the start and stop signals, said time-to-digital converter for digitizing the Δt time interval with reference to an off-chip precise reference clock.

2. The system of claim 1 further comprising valid event logic coupled with the time-to-digital converter, the valid event logic for rejecting invalid events.

3. The system of claim 1 further comprising a phase locked loop coupled with the time-to-digital converter, the phase locked loop for providing a time reference to the off-chip reference clock and to compensate for temperature and power supply variations.

4. The system of claim 1 further comprising adder logic coupled with the time-to-digital converter, the adder logic for correcting for timing offset.

5. The system of claim 1 wherein the output of the time-of-flight chip is an 11-bit linear word.

6. The system of claim 1 wherein the output of the time-of-flight chip is an 8-bit compressed word.

7. The system of claim 1 wherein original digital start and stop signals can be directly input to the time-to-digital converter bypassing the constant fraction discriminators.

8. The system of claim 1 wherein each constant fraction discriminator comprises:

an arming comparator having built-in hysterisis for avoiding multi-firing around a threshold), said arming comparator for receiving a positive input pulse wherein the arming comparator fires when the positive input pulse crosses a threshold;

a zero crossing comparator for receiving a delayed version of the positive input pulse and an attenuated version of the positive input pulse wherein the zero crossing comparator fires at a constant fraction of the positive input pulse; and

a logical AND gate coupled with a one-shot for receiving the output of the arming comparator and the zero crossing comparator, the AND gate and one-shot

providing a digital output for the constant fraction discriminator.

9. The system of claim 8 wherein each constant fraction discriminator further comprises an on-chip analog delay line.

10. The system of claim 1 wherein the time-to-digital converter comprises:

a time difference generating logic component for determining a start-stop time difference defined by the rising edges of two positive going signals ;

a time reference generating logic component for applying a train of negative going pulses from the reference clock to a calibration delay locked loop DLL;

a core of time-to-digital converter cells for receiving a valid negative going pulse of duration equal to the start-stop time difference wherein each cell truncates the valid negative going pulse by a fixed time; and

a position decoding component for determining the cell location where the valid negative going pulse disappeared.

11. The system of claim 10 wherein each time-to-digital converter cell is comprised of:

a current starving inverter; and

a standard inverter coupled with the current starving inverter,

such that a negative pulse of duration T entering a time-to-digital converter cell yields a negative output pulse with a controllable reduced duration.